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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,808	01/13/2004	Chaur-Chin Yang	JLINP143.DIV	5399

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EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 06/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/757,808	Yang	
	Examiner	Art Unit	
	Alexander Williams	2826	

-- The MAILING DATE of this communication app ars on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-6 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-6 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/293,123.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/757808 Attorney's Docket #: JLINP143.DIV
Filing Date: 1/13/2004; claimed foreign priority to 1/ 31/2002

Applicant: Yang

Examiner: Alexander Williams

This application is a divisional of serial # 10/293123, filed 11/12/2002.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 10/293123, filed on 11/12/2002. Claim 4 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 4 recites the limitation "the metal foil" in the signal tramsmission plate. There is insufficient antecedent basis for this limitation in the claim.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 to 6, **insofar as claim 4 can be understood**, are rejected under 35 U.S.C. § 103(a) as being unpatentable over Lin et al. (U.S. Patent # 6,509,646 B1) in view of Yamamura et al. (U.S. Patent # 4,949,224).

1. Lin et al. (figures 1 to 5) specifically figure 3 show a signal transmission plate **30**, the signal transmission plate comprising: at least one insulating layer **32**; at least one layout wire layer **31** formed on the insulating layer; and a solder mask **34** layer formed on the layout wire layer, the solder mask layer exposes partial area of the layout wire layer at the center and peripheries of the signal transmission plate to form a plurality of die bonding pads **42** and a plurality of wire bonding pads **41**, but fail to explicitly show a signal transmission plate used in a semiconductor package having a stacked die, a plurality of conductive wires, and a substrate.

(3) FIG. 3 is a cross-sectional view of an apparatus for reducing electrical noise inside a ball grid array package according to a second preferred embodiment of the present invention. The apparatus 21 of the second embodiment has two layers. The first layer is a contact layer 36 comprising the power plane 25 and the ground plane 24. A solder mask 34 is used to isolate the power plane 25 from the ground plane 24. The second layer is a signal layer 31 for transmitting electrical signals. The second layer is not limited to a particular material, such as copper. An insulating plane 32 is used to isolate the first layer from the second layer. The insulating plane is not limited to a particular material, and a BT resin can be used. The signal plane 31 is connected to the power plane 25 or ground plane 24 through vias 35 embedded a conductive material to achieve the function of signal transmission. The inside-connected capacitors 23 can be fixed on the

contact layer 36 by an adhesive glue 33, whose material is not limited. A red glue can be used as an adhesive glue. The inside-connected capacitors 23 can be electrically connected between the power plane 25 and ground plane 24 by a conductive glue 37, whose material is not limited. An alloy containing tin and lead can be used. The ground balls 22 and the power balls 27 with signal balls 26 are situated at both sides of the inside-connected capacitors respectively. It is important that the height of the inside-connected capacitors should be less than the height of the solder balls to avoid bad conductivity between the apparatus 21 of the second embodiment and the circuit board 13 due to insufficient conductive area.

Yamamura et al. is cited for showing a structure for mounting a semiconductor device. Specifically, Yamamura et al. (figures 1 to 6) specifically figure 1 show a stacked package comprising: a substrate **14** ; a first die **10b** electrically connected with the substrate; at least one signal transmission plate **8** provided on the substrate, the signal transmission plate including a plurality of die bonding pads **9,17** and a plurality of wire bonding pads **(9 on the end)**; at least one second die **10a** electrically connected to the die bonding pads; a plurality of conductive wires **12** for electrically connecting the wire bonding pads and the substrate; wherein the stacked die **10a** is electrically connected with the die bonding pads **9**, the wire bonding pads are electrically connected with the substrate **14** via the conductive wires **12** for the purpose of providing a structure for mounting a number of semiconductor devices on a circuit board without adversely affecting the characteristics of the individual devices.

3. The signal transmission plate as claimed in claim 1, Lin et al. show wherein the layout wire layer is formed by patterning a metal foil.

4. The signal transmission plate as claimed in claim 1, the combination with Lin et al. show wherein the metal foil is a copper foil.

5. The signal transmission plate as claimed in claim 1, the combination with Lin et al. show

wherein the insulating layer is formed by bismaleimide triazine (BT).

6. The signal transmission plate as claimed in claim 1,the combination with Lin et al. can be wherein the insulating layer is formed by glass epoxy since the insulating plane is not limited to a particular material.

Therefore, it would be obvious t one of ordinary skill in the art to use Yamamura et al.'s package assembly to modify Lin et al.'s signal transmission plate for the purpose of providing a structure for mounting a number of semiconductor devices on a circuit board without adversely affecting the characteristics of the individual devices.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/686,685,777,778,779,786,784,693,698,664,662,668, 678 174/250,255	6/9/04
Other Documentation: foreign patents and literature in 257/686,685,777,778,779,786,784,693,698,664,662,668, 678 174/250,255	6/9/04
Electronic data base(s): U.S. Patents EAST	6/9/04

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone

number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOW
6/10/04

Primary Patent Examiner
Alexander O. Williams